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Helping Struggling Data Centres to Handle Information
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The amount of data we are generating is increasing at a staggering rate. Unsurprisingly, the infrastructures we have in place to handle the information are becoming strained, posing serious threats to future data storage and processing capabilities. Dr Masum Hossain at the University of Alberta is working towards solving the issue, by increasing the efficiency of digital transmitters and receivers.

Data centres may be hidden from the public eye, but they are home to some of the most important computer systems in the world, including telecommunications networks and data storage facilities. With around 2.5 quintillion (2,500,000,000,000,000,000) bytes of data being generated every day as of August 2017 – a figure which only promises to increase – these facilities are now being forced to grow rapidly in both size and complexity, to keep up with the unrelenting flood of data.

Perhaps the most pressing issue is the problem of cooling. As computer systems operate, they generate enormous amounts of heat, which needs to be transferred away from the system to keep it functioning. Creating more complex and sophisticated cooling systems is crucial to keeping data centres operational, but the process is becoming increasingly difficult. Recently, a device has been proposed that could help to solve the ever-growing cooling problem.

A Serializer/Deserializer (SerDes) operates by converting data in the form of sequences of bits, transferred one at a time, into parallel signals, where multiple bits are sent at the same time. The devices are already used in high-speed communication systems, but if they are adapted for use in cooling systems, Dr Masum Hossain at the University of Alberta believes they could help to alleviate the issue of cooling efficiency.

THE DEATH OF MOORE’S LAW

Another concerning issue with data centres is their increasing struggle to become more compact – resulting from the breakdown of Moore’s law. First proposed by the founder of Intel, Gordan Moore, this law has been a steadfast prediction for technological advancement for much of computing history. Stating that the number of transistors in computer circuits will roughly double every two years, the rule has allowed companies and institutions to set targets and assess the progress of their increasingly compact systems over many decades. However, in more recent years, it has become clearer that end of Moore’s law is inevitable as CMOS scaling is expected to stop at a gate length of around a nanometre.

Ultimately, this means that the architectures of data centres become increasingly strained and outdated as the amount of data they are required to handle increases...
at a breakneck pace. However, Dr Hossain and his colleagues are now working towards creating devices that can handle more data at the same time, without the need for more transistors. In just a few years, the researchers have developed a wide variety of techniques to greatly reduce the power consumption in digital sequence converters, while increasing their speed, and ensuring as little data as possible is lost in the process.

A LOW-POWER DIGITAL SEQUENCE DETECTOR

In 2015, Dr Hossain and his colleagues described a technique for creating an energy-efficient device that could detect sequences of digital signals. In physical terms, data sequences are a series of waveform 'pulses', which carry information as they transfer between systems. Typically, pulses will interfere with the waveforms before and after them, which has long been a hindrance for digital detectors. In the past, techniques to deal with the interference have included reducing certain pulses, but this comes at the cost of increasing noise in the signal, limiting its performance.

In a new approach, the device created by Dr Hossain's team took advantage of the interference between pulses to reconstruct the digital signal in a time-dependent model. The researchers used a technique for decoding sequences in this way, which did not require conversion between analogue and digital systems – a process that requires high power consumption. After testing, the team found that their device consumed just 35 milliwatts in power, while detecting up to 10 gigabytes per second. At the same time, the system could compensate for signal loss due to interference, making it an attractive alternative for use as a low-power SerDes.

In a further study, Dr Hossain's team described a digital receiver that could efficiently modulate the amplitudes of signal pulses. For this, they adopted a pulse-amplitude modulator called PAM-4, and the associated signal-to-noise ratio penalty required the team to rethink the equalisation. Traditional symbol detection has signal-to-noise ratio limitations that requires a more sophisticated detection scheme. However, implementing them at such a high data rate significantly exceeds the power budget.

The conversion did mean that the power consumption of PAM-4 was higher than in the previous detector – an issue that the researchers hope to improve in future research. The team implemented PAM-4 using a semiconductor, which consumed 82 megawatts in power, but could handle up to 28 gigabytes per second – a significant improvement in efficiency.

REDUCING CHANNEL LOSS IN ANALOGUE-TO-DIGITAL CONVERSIONS

Dr Hossain's team adapted PAM-4 further in a 2018 study to create a digital receiver, which again used analogue-to-digital conversion, but also incorporated several new techniques to minimise signal losses in channels of data. The techniques included approximations of the waveforms' successive signal pulses in the channel, as well as a conversion of the signals from a time-dependent domain to a digital one. Like both previous devices, this version of PAM-4 took advantage of the interference between successive pulses – ultimately allowing for low error rates in bit signals, with little signal delay.

The researchers achieved the minimised channel loss using an impressively low number of electronic circuits, by allowing the circuits to be re-used continually. Overall, the device consumed 130 megawatts in power, while again processing 28 gigabytes of data per second. So far, this is the highest efficiency ever achieved for the levels of signal loss compensation demonstrated by Dr Hossain’s team – a promising prospect for the development of low-power SerDes in the near future.

HELPING DATA CENTRES TO COPE

Dr Hossain and his colleagues have successfully demonstrated how sophisticated techniques can be used to modify digital signal detectors and receivers – lowering their power consumption, while increasing their processing rates, and minimising signal loss. Their work will become increasingly important as the strain on data centres continues to increase. It will ensure requirements in cooling can be met using less power, and that slower progress in computer circuit advancements will still allow data centres to cope with the ever-increasing amount of data we produce.
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FURTHER READING
